a data buffer connected between the plurality of memory devices and the bidirectional data bus, the data buffer receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data buffer receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation, wherein the data buffer is shared by the plurality of memory devices.

REMARKS

Claims 29, 32, 38, 40, 42, 44, 48, 52, 63, and 67 are amended, no claims are canceled, and no claims are added; as a result, claims 5-8 and 29-71 remain pending in this application.

The claims are amended to clarify the recitations. It is not intended to restrict the scope to any significant extent that may surrender equivalents.

Drawing Objections

Applicant notes the objection to the drawings lacking reference number 120. Applicant above amends the specification to correct the reference number relating to the data bus to 115. Withdrawal of the objection to the drawings is requested.

The drawings were also objected to as lacking a data in buffer, a data out buffer, a column decoder, and a row decoder for the memory device (i.e., DRAM). Applicant herewith proposes a new Figure 6 showing these features. These features are part of the memory device as set forth in the specification. No new matter is believed proposed. Entry of new Figure 6 is requested.

Specification Objection

Applicant amends the specification, namely, the paragraph beginning on page 8 at line 3, as suggested by the examiner. No new matter is proposed. The specification amendment is supported by the drawings and the disclosure as a whole. Entry of the proposed specification amendment is requested.

Applicant further proposes amendments to specification paragraphs beginning on page 8, lines 18 and 27. Applicant amends these paragraphs to adopt a uniform reference number (115)

for the data bus and conform the reference number to the drawings.

Double Patenting Rejection

Claims 5-8 were provisionally rejected under the judicially created doctrine of double patenting over claims 1-4, 26-28, and 32-57 of Application No. 08/886,753. A Terminal Disclaimer will be considered when all claims are indicated to be otherwise allowable. Additionally, applicant requests clarification of the provisional status of this rejection.

§112 Rejection of the Claims

Claims 5-8 and 29-71 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant respectfully traverses. As described in MPEP § 2164 et seq., the following represents the *prima facie* case that the Examiner must provide in order to maintain a rejection of nonenablement with respect to the disclosure of a patent application under 35 U.S.C. § 112, first paragraph:

1. a rational basis as to
    a. why the disclosure does not teach, or
    b. why to doubt the objective truth of the statements in the disclosure that purport to teach;
2. the manner and process of making and using the invention;
3. that correspond in scope to the claimed invention;
4. to one of ordinary skill in the pertinent technology;
5. without undue experimentation; and
6. dealing with subject matter that would not already be known to the skilled person as of the filing date of the application.

Since the Examiner has not provided evidence supporting each of these elements, the Examiner has not made out a *prima facie* case for nonenablement under 35 U.S.C. § 112, first paragraph.

§103 Rejection of the Claims

Claims 5-8 and 29-71 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Katayama et al. (U.S. Patent No. 5,875,452). Applicant traverses.

The Examiner rejected the claims based only on Katayama. Applicant respectfully traverses the single reference rejection under 35 U.S.C. § 103 since not all of the recited elements of the claims are found Katayama. Since all the elements of the claims are not found in the Katayama, Applicant assumes that the Examiner is taking official notice of the missing elements. Applicant respectfully objects to the taking of Official Notice with a single reference obviousness rejection and, pursuant to M.P.E.P. § 2144.03, Applicant respectfully traverses the assertion of Official Notice and requests that the Examiner cite references in support of this position.

The examiner states that each element of the claims was either taught or suggested by the Katayama et al. reference alone (Office Action page 10). Applicant finds the examiner's statement puzzling as the examiner at Office Action page 5 admits that a data in and a data out buffer was not specifically mentioned in the Katayama et al. system. Clarification of these statements is requested.

As the examiner admits that Katayama et al. does not specifically mention a data in and a data out buffer, the examiner is relying on his statement that adding additional levels of buffer hierarchies was well known at the time the invention was made. Applicant respectfully traverses this assertion as a form of official notice as the examiner is relying on his assertion that adding levels of buffer hierarchies was well known at the time the invention was made. Applicant requests that the examiner provide a reference that describes such an element. Absent a reference, it appears that the examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). Applicant respectfully submits that the examiner's reliance on the fact that adding the additional buffers was well known actually is hindsight. The examiner has not applied any reference that shows all of the features of the present claims. Instead, the examiner is modifying Katayama et al. in an attempt to arrive at all of the features of the present claims. However, the justification set forth in the Office Action (page 5) is adding buffers to Katayama would have made timing of

the transfer operations to and from the shared buffers more efficient (by latching the data, control or address bits so that protocols as time sharing could be utilized), especially considering the highly parallel nature of Figure 9 embodiment of the Katayama et al system.

The Office Action further relies on St. Regis Paper Co. v. Bemis Co., 193 USPQ 8 (7th Cir. 1977) for a position that duplicate parts for multiple effects is not given patentable weight. Applicant does not see how St. Regis Paper applies to the present claims. First. Applicant requests that the "duplicate parts" relating to the present claims be identified. It appears that the examiner believes adding multiple storage devices 16 of Katayama et al. teaches all of the elements recited in the claims. Applicant respectfully traverses. Specifically, merely adding a plurality of Katayama's storage devices together does not teach or even suggest all of the elements of the claims. Specifically, Katayama does not teach or suggest the pipelined memory subsystems that each have a plurality of memory devices, wherein each contains a data in and a data out buffer, a column decoder and a row decoder, a command buffer and a data buffer as recited in claim 5. Further, the elements as recited in claim 5 do not rely on merely duplicating parts such as paper bag layers. The present invention as defined by claim 5 includes a plurality of memory subsystems, each connected to a controller through a command and address bus and a data bus. Each of the memory subsystems includes a plurality of memory devices, a command buffer and a data buffer. The system of claim 5 does not rely only multiple memory subsytems to distinguish over the art. The present system uses a unidirectional C/A bus and a data bus yet supports a plurality of devices per bus such that the total width of the data path width is not cost prohibitive to manufacture. For example, the present invention provides a memory system which utilizes a single 16-bit data bus which can be operated at 800 MHz and which supports 64 devices. Such a system can also be implemented as a higher bandwidth multiple data bus system as described in the specification. Accordingly, the present invention achieves effects beyond merely duplicating the memory systems.

Moreover, the feature of each memory device containing a data in and a data out buffer, a column decoder and a row decoder clarifies the recitations in the claims. Specifically, these components are in each memory device and that within the memory system an address buffer and a data buffer corresponding to a plurality of memory devices are in addition to the internal

components of each memory device because these features do, in fact, lend patentable weight. For example, the corresponding address buffer and data buffer result in an effect greater than the sum of the several effects taken separately. For example and as illustrated in Figure 1 of the present application, memory system 100 comprises N command and address buffers 131, N data buffers and N*M DRAMS. Each command and address buffer drives the latched command and address information to its corresponding plurality of memory devices. In this manner, the load on the C/A bus is reduced from N*M devices to only N devices. Additionally, the load on data bus 120 is reduced from N*M devices to only N devices. As a result the effects of the data in and data out buffer of each of the plurality of memory devices, in combination with the address buffer and the data buffer within the memory system are more than the sum of the single effects of the internal components of each of the plurality of memory devices. The addition of an address buffer coupled between a corresponding plurality of memory devices and a unidirectional command and address bus and a data buffer coupled between the corresponding plurality of memory devices and a bidirectional data bus results in a memory system which uses a single 16-bit data bus which can be operated at 800 MHZ and which supports 64 devices. In sum, the present invention as defined by the claims is not obvious under §103. And is certainly not analogous to the courts resolution in St. Regis interpretation of redundancy which found merely adding layers to a paper bag was obvious.

Based at least on the above, applicant submits that claim 5 is allowable. Additionally, claims 6-8 and 59-62 are believed allowable at least based on their dependance on claim 5.

Referring now to claim 62, it recites, the bidirectional data bus is a single 16 bit bus, supports 64 data buffers, and operates at 800 MHz. Applicant can not find these features in Katayama. Withdrawal of the rejection of claim 62 is respectfully requested.

Referring now to claim 29, applicant comments as follows. Claim 29 recites, in part, latching the data in the data in and data out buffer of the one of the plurality of memory devices and latching the data in the data buffer of the one memory subsystem. Applicant can not find these features in Katayama. Withdrawal of the rejection of claim 29 and claims 30-31 depending from claim 29 is respectfully requested.

Referring now to claim 32, applicant comments as follows. Claim 32 recites, in part, latching the data in the plurality of data buffers of the memory subsystem, driving the latched commands and addresses to the column and row decoders, and driving the latched data to the data in buffers of the memory device. Applicant can not find these features in Katayama. Withdrawal of the rejection of claim 32 and claim 33 depending from claim 32 is respectfully requested.

Referring now to claims 34-37 and 64 and claims 67-71, these claims are believed allowable for substantially similar reasons as stated above with regard to claim 5.

Referring now to claim 38, applicant comments as follows. Claim 38 recites, in part, if the memory transaction is a write, receiving and latching the data in the data buffers of the plurality of memory subsystems, driving the latched data to the data in and data out buffer, and writing the data to an addressed memory storage of the plurality of memory devices. Applicant can not find these features in Katayama. Withdrawal of the rejection of claim 38 and claim 39 depending from claim 38 is respectfully requested.

Referring now to claim 40, applicant comments as follows. Claim 40 recites, in part, latching the data received from the bidirectional data bus in the data buffers of the plurality of memory subsystems, driving the latched commands and addresses to the plurality of memory devices, driving the latched data to the data in and data out buffer of the plurality of memory devices, and storing the data from the data in and data out buffer in addressable storage of the plurality of memory devices. Applicant can not find these features in Katayama. Withdrawal of the rejection of claim 40 and claim 41 depending from claim 40 is respectfully requested.

Referring now to claim 42, applicant comments as follows. Claim 42 recites, in part, retrieving data from addressable storage of the plurality of memory devices of the plurality of memory subsystems, latching the data in the data in and data out buffer of a memory storage device, and latching the data in the data buffers of the plurality of memory devices of the plurality of memory subsystems. Applicant can not find these features in Katayama. Withdrawal of the rejection of claim 42 and claim 43 depending from claim 42 is respectfully requested.

Referring now to claim 44, applicant comments as follows. Claim 44 recites, in part, a data buffer connected between the plurality of memory devices and the bidirectional data bus, the

data buffer receiving and latching data information from the bidirectional data bus and driving the data information to data in and data out buffer of the plurality of memory devices for a write operation, the data buffer receiving and latching the data information from the data in and data out buffer of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation. Applicant can not find these features in Katayama. Withdrawal of the rejection of claim 44 and claims 45-47 and 65 depending from claim 44 is respectfully requested.

Referring now to claim 48, applicant comments as follows. Claim 48 recites, in part, latching the commands and addresses in the plurality of command buffers, latching the data in the plurality of data buffers, driving the latched commands and addresses to the column and row decoders, driving the latched data to the data in buffers, and storing the data latched in the data in buffer in the addressable storage of the plurality of memory devices. Applicant can not find these features in Katayama. Withdrawal of the rejection of claim 48 and claim 49 depending from claim 48 is respectfully requested.

Referring now to claim 50, applicant comments as follows. Claim 50 recites, in part, latching the data in the data in and data out buffer of the memory device, latching the data from the data in and data out buffer in the plurality of data buffers, and driving the data from the data in and data out buffer onto a data bus. Applicant can not find these features in Katayama. Withdrawal of the rejection of claim 50 and claim 51 depending from claim 50 is respectfully requested.

Referring now to claim 52, applicant comments as follows. Claim 52 recites, in part, a data buffer connected between the data in and data out buffer of each of the plurality of memory devices and the bidirectional data bus, the data buffer receiving and latching data information from the bidirectional data bus and driving the data information to the data in and data out buffer of the plurality of memory devices for a write operation, the data buffer receiving and latching the data information from the data in and data out buffer of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation. Applicant can not find these features in Katayama. Withdrawal of the rejection of claim 52 and claims 53-55 and 66 depending from claim 52 is respectfully requested.

Referring now to claim 63, applicant comments as follows. Claim 63 recites, in part, retrieving data from addressable storage of one of the plurality of memory devices, latching the data in the data in and dat out buffers, latching the data from the data in and data out buffer in the data buffers, and receiving the data on the bidirectional data bus. Withdrawal of the rejection of claim 63 is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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